

A circuit model for the post-breakdown I-V characteristics in MOS devices on P-type substrate

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Abstract

The post-breakdown leakage current in MOS p-silicon devices cannot be modeled with a single-diode and a series resistance for the complete range because of the complex shape of its logarithmic plot. For low voltage, the current can be described by a single-diode model and a series resistance, and for high voltage a different single-diode model and a resistance can be used. These two regional single-diode models are combined in a double diode model with two resistances.

Keywords: Oxide breakdown, metal-oxide-semiconductor, reliability.

Modelo circuital de la corriente de post-ruptura en dispositivos MOS con sustratos tipo P

Resumen

La corriente de fuga de post-ruptura en dispositivos de silicio MOS con sustrato tipo p no puede ser modelada con un solo diodo y una resistencia en serie en todo el rango debido a la complicada forma de la gráfica logarítmica. Para bajo voltaje, la corriente se puede describir con un sólo diodo y resistencia, y para alto voltaje otro diodo y resistencia deben usarse. Estos dos modelos diferentes pueden combinarse en un solo modelo con dos diodos y dos resistencias.

Palabras clave: Ruptura del oxido, metal-oxido-semiconductor, confiabilidad.

1. INTRODUCTION

Modeling the Post-Breakdown *I-V* characteristics in MOS devices has been studied recently [1-7] as a possible way to obtain information about the reliability of these devices. Several attempts have been made to understand the post-breakdown conduction mechanism and to model the *I-V* characteristics under this condition. A simple model, based on an ideal diode with a series resistance as illustrated in Figure 1, was proposed recently [1-3] for MOS devices on n-type silicon substrate.

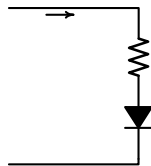


Figure 1. Equivalent circuit for the breakdown path in MOS devices on n-type substrate.

The *I-V* characteristic of the equivalent circuit presented in Figure 1 for MOS devices on n-type substrate is defined by:

$$I = I_0 \left\{ \exp \left[\frac{V - I R}{n V_{th}} \right] - 1 \right\} \quad (1)$$

where *I* is the terminal current, *V* is the terminal voltage, *R* is a resistance, *I*₀ is the reverse saturation current, *n* is the ideality factor, and *V*_{th} = *kT*/*q* is the thermal voltage.

The analytic solution of *I* and *V* from this equation yields [8, 9]:

$$V = I R + n V_{th} \ln \left(\frac{I + I_0}{I_0} \right) \quad (2)$$

$$I = \frac{n}{R} \frac{V_{th}}{V_{th}} W \left\{ \frac{I_0 R}{n V_{th}} \exp \left[\frac{(V + I_0 R)}{n V_{th}} \right] \right\} - I_0 \quad (3)$$

where W is the principal branch of the Lambert function [10, 11]. For this case the parameters can be extracted using several methods [12-15].

In this paper we show that modeling the post-breakdown current in MOS devices on p-type substrate is more complicated than that of devices on n-type substrate [1, 2]. In fact, these I-V characteristics need to be modeled with a combination of two diodes and two resistors.

2. MODELING AND MEASUREMENTS

For the experiments we used standard MOS capacitors grown on 1-12 Wcm n- and 4-40 Wcm p-type Si substrates with 350 nm thick n+doped poly-Si gate deposited by Liquid Phase Chemical Vapor Deposition (LPCVD), using POCl₃ diffusion at 900 °C, and oxide thicknesses of 3.8, 4.3, and 4.9 nm. The samples were subjected to ramped voltage stress in the high integration mode until the detection of the first hard breakdown (HBD) event.

Figure 2 presents the measured current-voltage characteristics for a capacitor grown on p-type Si with a gate oxide thickness of 4.9 nm at room temperature (25 °C). The shape of this logarithmic plot cannot be simulated with a single-diode model for the complete range.

Nevertheless, a single-diode model can be used to obtain a good fit of the experimental data for the low voltage region ($0 < V < 0.6$ V) and a different single-diode model can also be used to obtain a good fit for the high voltage region (0.6 V $< V < 2.0$ V). Figure 2 also presents these two regional fits using $n=1$, $I_0=5 \times 10^{-12}$ A and $R=100$ KΩ for the low voltage region, and $n=3.3$, $I_0=5 \times 10^{-10}$ A and $R=2$ KΩ for the high voltage region.

A possible single model, valid for the complete region, is presented in Fig 3. This model is inspired in joining in one circuit two different single-diode models. The diodes D_1 and D_2 present different ideality factors, n_1 and n_2 , and different reverse saturation currents, I_{O1} and I_{O2} respectively.

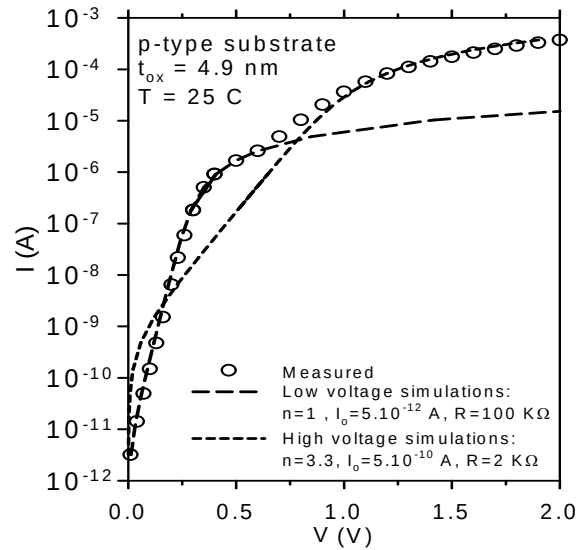


Figure 2. Post-breakdown I-V characteristics for a capacitor grown on p-type Si with a gate oxide thickness of 4.9 nm at T=25 °C and two regional fits for the low and the high voltage regions.

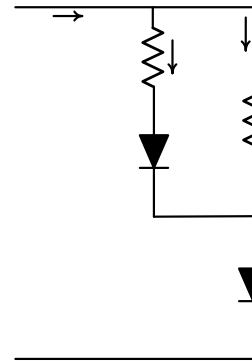


Figure 3. Equivalent circuit for the breakdown path in MOS devices on p-type substrate

The parameter values are selected such that for low voltage, the current in resistor R_1 is negligible compared to the current in R_2 . Therefore, the current at low voltage is mainly defined by the combination of D_2 and R_2 . At high voltage the current in resistor R_2 is much smaller than that of R_1 . Then, for high voltage, the main path of conduction is through the series combination of R_1 , D_1 and D_2 . Figure 4 presents AIM-SPICE [16] simulations of this circuit showing the total current I and its two components I_{R1} (the current in resistor R_1) and I_{R2} (the current in resistor R_2). In this simulation we have used the following parameters: $n_1=2.2$, $I_{O1}=4.86 \times 10^{-9}$ A, $R_1=2.64$ KΩ, $n_2=1.02$, $I_{O2}=3.73 \times 10^{-12}$ A and $R_2=94.7$ KΩ. We see in this

figure that I_{R2} dominates at low voltage, while I_{R1} dominates at high voltage.

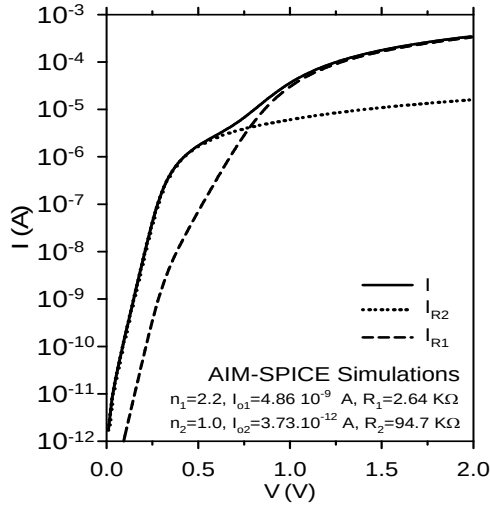


Figure 4. AIM-SPICE simulations showing the total current I and its two components I_{R1} (the current in resistor R_1) and I_{R2} (the current in resistor R_2).

A series combination of two ideal diodes can be modeled [17] at high voltage by a single effective diode having:

$$n_{HV} = n_1 + n_2 \quad (4)$$

$$I_{OHV} = n_{HV} \sqrt{I_{O1}^{n1} I_{O2}^{n2}} \quad (5)$$

where n_{HV} and I_{OHV} are the effective ideality factors and reverse saturation currents for high voltage. Therefore, the current at high voltage is mainly defined by the series combination of R_1 and the effective diode D_{HV} , which has n_{OHV} and I_{OHV} . Using the parameters values in Figure 4, equation (4) implies $n_{HV}=3.3$ and equation (5) yields to $I_{OHV}=9.88 \times 10^{-10}$ A. These two values are very close to the high voltage regional approximation illustrated in Figure 2.

A complete nonlinear optimization of all the parameters can be done and the results for this case is: $n_1=2.2$, $I_{O1}=4.86 \times 10^{-9}$ A, $R_1=2.64$ KΩ, $n_2=1.02$, $I_{O2}=3.73 \times 10^{-12}$ A and $R_2=94.7$ KΩ. These values can be used to obtain the previous low and high voltage approximate models by using equations (4) and (5). The simulated and the experimental results for two temperatures are illustrated in Figure 5. The good fit between experimental and simulated data indicates that the two-diode model is adequate to describe the

post breakdown conduction in capacitors grown on p-type Si. The physical origin of this new approach remains to be investigated.

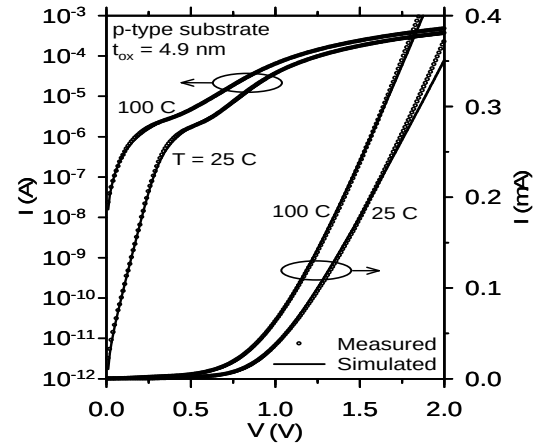


Figure 5. Post-breakdown I-V characteristics for a capacitor grown on p-type Si with a gate oxide thickness of 4.9 nm at $T=25$ C and $T=100$ C.

This procedure was used for temperatures ranging from 25°C to 100°C. The temperature dependences of the extracted parameters are presented in Figure 6. We observed that I_{O2} increases with temperature and that the other parameters are weakly dependent on temperature.

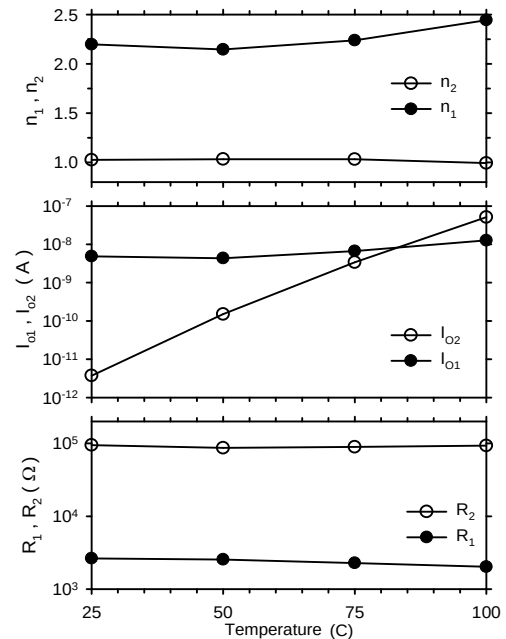


Figure 6. Parameters extracted using nonlinear optimization. The effect of diode D_2 is negligible for $T > 100$ C and thus the parameters n_2 and I_{O2} are not extracted above this

3. CONCLUSIONS

The post-breakdown leakage current in MOS p-silicon devices cannot be modeled for the complete range with a single-diode and a series resistance. Two regional approximations, for low and high voltage, can be used based on a single-diode model and a series resistance. These two regional models are combined in a double diode model with two resistances. This new circuit model is valid for all regions of operation.

4. REFERENCES

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